Waveguide Formation through Post-foundry Processing using Patterned Shallow Trench Isolation of CMOS Die
Technology #16489

Applications

- Communication transceivers
- Application specific integrated circuits requiring electronic-photonic integration
- Integrated quantum optics
- Integrated photonic biosensing
- Optical I/O

Problem Addressed

Optical I/O resolves one of the major bottlenecks in inter and intra chip communications. However, creating waveguides for photonic-electronic devices in bulk semiconductor manufacturing process requires complicated post-processing and high-resolution lithography, which is very costly. Alternatively, back-end integrated waveguides are physically distant from the transistor body layer, making integration with silicon photodetectors, etc., difficult. Deposited dielectric layers also reduce the thermal conductance of the entire chip, reducing allowable power dissipation and hindering performance.

Technology

The invention utilizes shallow trench isolation features patterned during in-foundry processing for subsequent waveguide formation via a post-process dielectric deposition. This is accomplished after etching the silicon on the back side of the wafer and then exposing the photonic integration region, where the desired photonic waveguide core dielectric layer is uniformly deposited, and finally depositing a lower cladding dielectric layer on the waveguide cores. This process is entirely CMOS compatible and utilizes standard patterning and etching techniques.

Advantages

- Low-loss, high patterning resolution waveguide within electronics process utilizing bulk starting wafers
- Waveguide in-plane with transistor body layer allows coupling to other electronic/photonic devices
- Standard CMOS process flow
- Improved waveguide integration for wavelengths covering 400nm – 1150 nm with arbitrary dielectrics
- Reduced dielectric covering of die or wafer, which increases total allowable power dissipation

Categories For This Invention:

Electronics & Circuits
Semiconductors & Integrated Circuits
Semiconductor Manufacturing

**Intellectual Property:**

Waveguide formation using CMOS fabrication techniques
Issued US Patent
9,529,150
Waveguide formation using CMOS fabrication techniques
Issued US Patent
9,946,022
Waveguide formation using CMOS fabrication techniques
Issued US Patent
Waveguide formation using CMOS fabrication techniques
US Patent Pending

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**Publications:**

Silicon Photonics Meets the Foundry
ILP News
June 22, 2015

**External Links:**

Physical Optics & Electronics Group
http://www.rle.mit.edu/sclaser/
Research Laboratory of Electronics
http://www.rle.mit.edu/

**Image Gallery:**

![Image of wafer]