3D Cryogenic Packaging for Superconducting Computing
Technology #19039

Applications

Superconducting computing offers an attractive low-power alternative to CMOS. Cryogenic packaging with 3D integration will allow superconducting computer circuits to fit within cryogenic chambers.

Problem Addressed

In the realm of computing, superconducting integrated circuits greatly outperform CMOS with many advantages including faster switching speeds, low dissipative switching, and the use of small current pulses for information transfer. The major challenge is the lack of existing high performance integration schemes that meet the stringent requirements of cryogenic applications. Current technologies cannot provide an integration scheme that accommodates the thousands of single flux quantum chips needed for operation. Other requirements include high integration density per chip, a substantially miniaturized cryogenic cooling setup, low-resistance signal paths, and stability over cryogenic temperature ranges.

Technology

A superconducting computing architecture with a scalable cryogenic 3D integration approach is the solution to these requirements. This approach yields the ability to design computing circuitry to fit the cryogenic space, rather than adjusting the cryogenic space to fit the computer circuits. The cryogenic package includes multiple superconducting multi-chip modules, which connect to each other with room temperature semiconductor components. This structure allows the selection of the best possible, commercially available, superconducting die and components from various suppliers. The 3D design minimizes the use of physical space, and maximizes superconducting paths, to increase processing speeds and decrease signal path resistance.

Advantages

- 3D cryogenic integration approach shrinks superconducting computing hardware to small enough area to fit in cryogenic chamber
- Decreased electrical resistance in signal path, increased processing speed

Related Technologies

This technology is related to 18087 – Low Loss Superconducting Integrated Circuits, and 18282 – Cryogenic Qubit Integration

Categories For This Invention:
Electronics & Circuits
Semiconductors & Integrated Circuits
Design & Fabrication
Superconductors
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Intellectual Property:
Interconnect structure and semiconductor structures for assembly of cryogenic electronic packages
Issued US Patent
Cryogenic electronic packages and assemblies
Issued US Patent
Cryogenic electronic packages and methods for fabricating cryogenic electronic packages
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Publications:
Large-Scale Cryogenic Integration Approach for Superconducting High-Performance Computing
IEEE 67th Electronic Components and Technology Conference
2017
Cryogenic Qubit Integration for Quantum Computing
IEEE 68th Electronic Components and Technology Conference
2018

External Links:
Lincoln Laboratory
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