MIT TLO Technology Licensing Office

Cryogenic Qubit Integration

Technology #18282

Applications

Superconducting circuits are most prevalently used in large-scale quantum computing. Since superconductor materials have substantially no electrical resistance below a certain critical temperature, they provide increased performance in integrated circuit devices, which can be used in a variety of electronic devices.

Problem Addressed

To achieve the high computation speeds that meet the demands of higher functionality in integrated circuits while being pushed into smaller footprints, new packaging structures need to integrate more dies with greater function, higher I/O counts, and smaller die pad pitches. The current solutions for densifying packages are based upon materials selection, package design, and integration approach. This technology identifies material selection, package design, and integration approaches to minimize resistance for a superconducting path between two chips in a flip-chip configuration.

Technology

This technology is a cryogenic bit package comprised of quantum bit integrated circuits, a quantum bit bias control line, a superconducting multi-chip module, and superconducting interconnects to electrically couple the qubit circuits to the multi-chip modules. The interconnect structure is formed on a semiconductor structure with a resistive substrate and an interconnect pad, which together, allow for assembly of multi-layer semiconductor structures with multiple superconducting integrated circuits. This multi-layer semiconductor structure has a series of coupled interconnect sections that use superconducting qubit ICs to perform fast and nearly loss-less operations for quantum computer architectures. The interconnects of this system demonstrate minimal resistance in the superconducting path as well as efficient heat dissipation in the thermally conducting path.

Advantages

- Stable interconnect with room temperature electronics.
- Increased I/O density for multi-qubit operations. Constitutive layer geometry supports long coherence times

Related Technologies

This technology is related to 18087 – Low Loss Superconducting Integrated Circuits, and 19039 – 3D Cryogenic Packaging for Superconducting Computing

Categories For This Invention:

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Electronics & Circuits
Semiconductors & Integrated Circuits
Design & Fabrication
Superconductors
Lincoln Laboratory

Intellectual Property:

Interconnect structures and methods for fabricating interconnect structures
Issued US Patent
Qubit and coupler circuit structures and coupling techniques
Issued US Patent
Shielded through via structures and methods for fabricating shielded through via structures
Issued US Patent
Interconnect structures for assembly of semiconductor structures including superconducting integrated circuits
Issued US Patent
Interconnect structures and methods for fabricating interconnect structures
PCT
2017-079394
Qubit and coupler circuit structures and coupling techniques
PCT
2017-131831
Interconnect structures for assembly of semiconductor structures including superconducting integrated circuits
PCT
2017-079417
Shielded through via structures and methods for fabricating shielded through via structures
PCT
2017-079424

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Publications:

Large-Scale Cryogenic Integration Approach for Superconducting High-Performance Computing
IEEE 67th Electronic Components and Technology Conference
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Cryogenic Qubit Integration for Quantum Computing
IEEE 68th Electronic Components and Technology Conference
2018

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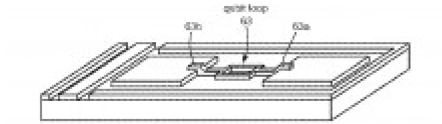

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