Interconnect Structures for Assembly of Multi-Layer Semiconductor Devices  
Technology #17313

Applications

This interconnect technology is applicable to multi-layer semiconductor devices. Multi-layered devices can be used in military and commercial applications. This includes sensor processing, data recording, communication, and flight electronics. On the commercial side, this is applicable to portable consumer electronics like cell phones, tablets, and laptops.

Problem Addressed

There is a trend toward miniaturization of electronic products in mobile phones, tablets, and digital cameras. Consequently, there is a trend in semiconductor device manufacturing towards smaller and more densely packed semiconductor structures. This has resulted in a demand for semiconductor packages which are relatively low loss, lightweight structures and which support increased electronic capabilities (e.g., increased density, mobility and extended operational life) in miniaturized electronic products demanded by both military and commercial customers alike. The foregoing trend and demand, drives a need for multi-layer semiconductor devices, semiconductor devices including at least two semiconductor structures. There is consequently, a need for interconnect structures which enable assembly of multi-layer semiconductor devices.

Technology

A miniaturized 3DIC integrated electronic package has multiple functional sections attached to each other through oxide bonding where each section can have single or multiple layers. Micro vias confined within opposing layers, interconnect between layers of each functional section. The vias may have variable diameter from top to bottom to maximize space efficiency. The 3DIC package can also be attached to multi-chip modules through microbumps or pillar technology. Instead of microbumps, a third via can be used to make electrical connection between two stacks where the third via is a high CTE metal with equal or larger size and pitch than the second micro via. The materials stack-up for each functional section may vary but at least one functional section will contain one active transistor layer and two local interconnect routing layers for each active transistor layer. The bonding of multiple functional sections allows the mixture of III-V transistors with Silicon CMOS, for example.

Advantages

- Enhanced system capabilities as well as reduced size, weight, power, and cost
- Significant reduction in the length of metal interconnect lines yielding increased circuit speed, decreased power loss
- Increased freedom in mixing technologies and materials without compromising performance, widening the design space for this device
- Eliminates the need for through silicon via, decreased chip fragility
Increased Package-on-Package (PoP), embedded active circuit densities
Presents the possibility for use in wafer level packaging (WLP)

Related Technologies


Categories For This Invention:

Electronics & Circuits
Semiconductors & Integrated Circuits
Design & Fabrication
Lincoln Laboratory

Intellectual Property:

Semiconductor structures for assembly in multi-layer semiconductor devices including at least one semiconductor structure
Issued US Patent
Interconnect structures for assembly of multi-layer semiconductor devices
Issued US Patent
9,780,075
Interconnect structures for assembly of semiconductor structures including at least one integrated circuit structure
Issued US Patent

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