Interconnect Structures for Fine Pitch Assembly of Semiconductor Structures
Technology #16918

Applications

This interconnect technology was designed to support military applications, however, the devices may support the miniaturization of electronic products such as mobile phones, tablets, and digital cameras while providing enhanced sensor processing and communication performance.

Problem Addressed

Today’s military and commercial electronics demand increased density, enhanced mobility, and extended operational life. In addition, new electronic packages require low loss, lightweight structures, higher electrical performance, and mixed material construction with the structural stability to accommodate the complexity associated with size, weight and power optimization. This requires the integration of multiple interconnected structures, yielding die with greater function, higher I/O counts and smaller pitches. While it is desirable to reduce interconnect pitch, relatively simple and cost effective approaches are needed in order for such a technology to be practical. Current conventional interconnects, such as solder pads, self-aligned contact pads, bond wires, and conductive pads, are bulky and their associated pitch is not easily reduced. This results in a less effective use of the space on the integrated circuit and a less powerful circuit overall.

Technology

The presented technology reduces interconnect width, allowing a reduced pitch in comparison to conventional semiconductor structures and devices. This is accomplished with a semiconductor structure composed of a substrate, interconnect pad, and an isolating layer where one or more conductive structure projecting from the surface of an interconnect pad form a connection for electrically and mechanically coupling the semiconductor structure to other semiconductor structures and devices. The electrical connections may be made by drilling holes through the substrate in appropriate locations and plating the inside of the holes with a conducting material (e.g., copper). The interconnect pad is provided to promote scalability of the semiconductor structure since it can couple to other semiconductor structures or devices. An isolating layer includes a polymer, which may be used as a dielectric bridge for crossover of circuits within the same layer of substrate. This dielectric bridge may be created by selective deposition of a dielectric material (e.g., nanoporous silica, silicon oxyfluoride) using physical or chemical vapor deposition. Openings in the isolating layer may be formed by an additive or subtractive process which accommodates one or more conductive structures that fits between the interconnect pad and isolating layer. These processing conditions are cheaper and less bulky than conventional methods of reducing pitch size.

Advantages

- Shortens assembly and package construction times
- Improved RF performance due to conversion to flip-chip from wire bondable package
• Reduced pad size and spacing to convert standard substrates to finer pitch substrates
• Reduced total interconnect resistance, less power dissipation

Related Technologies

This technology is related to: 17313 – Interconnect Structures for Assembly of Multi-Layer Semiconductor Devices, 17465 – Interconnect Structures for Assembly of Multi-Layer Semiconductor, and 18705 – Multi-Layer Semiconductor Structure

Categories For This Invention:

Electronics & Circuits
Semiconductors & Integrated Circuits
Design & Fabrication
Lincoln Laboratory

Intellectual Property:

Interconnect structures for fine pitch assembly of semiconductor structures and related techniques
Issued US Patent
9,786,633

Inventors:

Rabindra Das
Peter Murphy
Karen Magoon
Noyan Kinayman
Michael Barbieri
Timothy Hancock
Mark Gouker

External Links:

Lincoln Laboratory
https://www.ll.mit.edu

Image Gallery: