Improved Enhancement of P-type/N-type Metal-Oxide-Semiconductor Field Effect Transistors Preserved over a Large Processing Temperature Range
Technology #10578

Applications

This technology can be applied to various electrical devices such as metal-oxide-semiconductor field-effect transistors (MOSFETs).

Problem Addressed

There is need for higher currents in MOSFETs.

Technology

This invention consists of a tri-channel hetero-structure which has a tensile strained semiconductor layer, a compressively strained layer and a confining layer. The thicknesses and doping concentrations of the first two layers are optimized for wide ranges of performance enhancement. The third layer has a band offset with the second layer to confine carriers, and provides a diffusion barrier to the second layer over a large temperature range. A gate dielectric could be disposed over the first, the second or the third layer to form a MOSFET. A method of forming the above structure is also provided.

Advantages

- High hole and electron mobilities
- High performance over a large processing temperature range

Categories For This Invention:

- Electronics & Circuits
- Electronic Components
- Power Transistors

Intellectual Property:

Strained tri-channel layer for semiconductor-based electronic devices
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FIG. 1