Control of Current Collapse in Thin Pattern GaN
Technology #18476

Applications

High electron mobility transistors (HEMTs) are suitable for high power, high frequency and/or high temperature applications.

Problem Addressed

HEMT efficiency is limited by a current collapse phenomena in Gallium Nitride (GaN) metal-semiconductor field effect transistors. Current collapse occurs when the GaN on-resistance increases and current decreases during the application of high voltage to the device. Pronounced current collapse (40% or greater) in C-doped GaN HEMTs is observed when the GaN buffer layer is < 2 microns. This technology uses metal organic chemical vapor deposition (MOCVD) to create a patterned region between GaN and the substrate to reduce current collapse.

Technology

This technology uses a silicon on insulator (SOI) substrate. During co-integration of GaN with 200 mm hybrid SOI, patterned regions are created such that <111> Si is exposed. The depth and coverage of the patterned region cannot exceed 1.5 µm and 50%, respectively, because it will create large stresses during GaN growth on the Si. The SOI substrate thickness is typically in the range of 725-775 µm and corresponds to that used by Si CMOS industry. The invention demonstrates how the current collapse can be reduced to <10% even with <1.5 µm GaN HEMT structure in the patterned region.

Advantages

• Reduces current collapse
• Improves HEMT performance

Categories For This Invention:

Electronics & Circuits
Electronic Components
Power Transistors
Semiconductors & Integrated Circuits
Semiconductor Manufacturing

Intellectual Property:

Control of current collapse in thin patterned GaN
Issued US Patent
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Publications:
GaN Devices on a 200 mm Si Platform Targeting Heterogeneous Integration
IEEE Electron Device Letters
vol.38, no.8, pp.1094-1096, Aug. 2017

External Links:
Palacios' Group
http://www-mtl.mit.edu/wpmu/tpalacios/