CMOS Readout Circuit Architecture for Large-format Small-pixel Photon Counting Focal Plane Arrays Using Geiger-Mode Avalanche Photodiodes
Technology #13765

Applications

The invention is useful for medical and defense applications (night vision, remote surveillance, adaptive optics and bio-detection); quantum computing; cryptography and information technology; scientific imaging; and imaging for the consumer markets.

Problem Addressed

Current CMOS architecture with one-bit sensing requires a lot of real estate thus limiting the minimum size and spatial resolution of the image. There is a need for photon-counting imagers with low transfer bandwidths, relatively small sensing elements, and high dynamic range.

Technology

The invention is a complementary metal-oxide-semiconductor (CMOS) readout architecture for photon-counting imagers which include an array of sensing elements, each of which includes a photon-counting detector, such as an avalanche photodiode (APD) operating in Geiger mode, a digital counter, and an overflow bit. Typically, the photon-counting detector is a Geiger-mode avalanche photodiode (APD) that emits brief pulses every time it detects a photon. The pulse increments the digital counters, which, in turn, sets the overflow bit once it reaches a given count. A rolling readout system coupled to each sensing element polls the overflow bit, and, if the overflow bit is high, initiates a data transfer from the overflow bit to a frame store.

Advantages

- CMOS architectures with counters and overflow bits have lower transfer bandwidths, higher dynamic ranges, and dissipate less power when compared to other CMOS architectures
- Smaller in size
- Cheaper to make
- Better spatial resolution.

Categories For This Invention:
Lincoln Laboratory
Photonics
Sensors (Photonics)
Life Sciences
Imaging
X-ray, CT, PET

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